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EXAMINER	
NGUYEN, MATTHEW VAN	
ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 08/20/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/561,735	12/20/2005	Jan Dikken	GB30100US1	7773

TITLE OF INVENTION: DEAD TIME CONTROL IN A SWITCHING CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1440	$300	$0	$1740	11/20/2008

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

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(Depositor's name)

(Signature)

(Date)

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10/561,735	12/20/2005	Jan Dikken	GB30100US1	7773

TITLE OF INVENTION: DEAD TIME CONTROL IN A SWITCHING CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1440	$300	$0	$1740	11/20/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, MATTHEW VAN	2838	323-271000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

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Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee

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☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

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☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

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DATE MAILED: 08/20/2008

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 394 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 394 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	10/561,735	DIKKEN ET AL.	
	Examiner	Art Unit	
	MATTHEW V. NGUYEN	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed on 6/17/08*.

2. ☒ The allowed claim(s) is/are *1-18*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
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4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

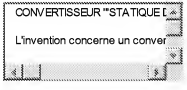
1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/MATTHEW V NGUYEN/
Primary Examiner, Art Unit 2838

1. The following is an examiner's statement of reasons for allowance: besides the response including arguments in the Remarks of Applicant filed on 6/17/08, the translation into English of the document FR 2 680 056 is attached hereto, in which there is no limitations of means for adjusting the length of a dead time period according to a voltage difference between the drain and the source of the first or second transistor.

2.

Translation: French » English



CONVERTER "STATIC ELECTRIC POWER SEMICONDUCTOR

The invention relates to a static electric energy to semiconductors. It is a converter with two switches static type'-ordered to boot and blocking the terminals which are connected to antiparallel diodes, sometimes referred to as "diodes coasting" (which will ensure the free movement of the load current in case of simultaneously blocking two switches). This structure converter is especially used for UPS or voltage converters resonance.

The invention includes a converter Basic including two switches and converters made more complex by combining these basic converters (each of which is generally designated in this case by "arm of UPS").

There are essentially two types of converters with the structure above: one running commutation described as "tough" in which the commutations switches are independent of the sign of current through the load, the other running commutation "soft" in which commutations are made taking into account the sign of this trend in order to avoid a violent stalemate diodes coasting, which could lead to surge, surge and losses ...

In the first type converter, it usually avoids the simultaneous conduction of the two switches (which entails a short-circuit the source of tension) by introducing a time delay (known as "time-out") between the blocking of a switch and boot on the other. This time out, sets in most montages, is sometimes adapted to the

conditions of operation so as to minimize and avoid short-circuits (reference: J. BARRET, Thomson Semiconducteurs France, "Interactive switching in a bridge leg" EPA '87 Grenoble; S. BONTEMPS, Compact Power SA, "Module hybrid power for the control and protection arm of UPS bipolar

1000V/1000A. "," Electronic Power of the Future, Toulouse,

October 1990), in the case of a bipolar technology

(bipolar transistors), the logical command converter is then carried out by detecting the state of polarization of the junction base / issuer of a bipolar transistors and prohibiting booting the switch if the complementary junction east conductive . This improvement avoids short-circuits the source of tension but does not include violent blockades of diodes coasting. Moreover, this technique is di ficilement transposable outside a bipolar technology.

The U.S. patent 4,641,231 and patent 4,038,299 OF describe such devices that can prevent short circuits in the arm inverter but unable to remove the risk of violent blockades of diodes coasting: these devices, the state of the additional switch is detected at its electrode command, but in no case is taken into account the state blocked or passing diodes coasting. It is noteworthy that in option represented in Figure 6 of U.S. patent 4,641,231, is added so redundant detection of the state or blocked from the switch complementary to seek the best moment of initiation; this detection, which doubles the detection made at the electrode order is ensured on electrodes that power switch (comparator 82) and the detection signal is combined with a signal of current information (from comparator 90) give a specific logic to obtain a redundancy command switches in order to avoid short-circuit such an arrangement is totally unsuited to remove blockages of violent diodes coasting. In addition, the converters of the second type (operating commutation soft) have a logical order that takes into account the sign of the current load: they are, therefore, crucial advantage to exclude violent blockades diodes and their injurious consequences, it is worth noting that for a

switch given the reduction in losses by switching allows operating frequencies much higher. In addition, subject to specific commutation logic, some montages of this second type also exclude the risk of short-circuiting the source of tension *. (patent FR 78/32428). However, these arrangements will have a number

of defects due precisely to their logical commutation very constraining: this logic prohibits, in effect, commutations to load current void and therefore requires at start-up, an auxiliary device to initiate specific operation; furthermore, in the vicinity of operations to empty, this logic leads to stops that require the addition of auxiliary circuits forcing commutation (patent FR 85/16894). In other words, the logical command converters this second type provides an ideal security commutation but implies a significant reduction of the operating range: to expand again this beach, it becomes necessary to modify the power circuits , With additional costs high.

This invention is to provide a new converter commutations fresh, free of defects mentioned above, which removes both the risks of short circuits and violent blockades of diodes coasting. The invention is designed especially to help meet simultaneously the following advantages:

-- Commutation excluding fresh opportunities for violent blockades of diodes coasting, each accompanied by switching overcurrent surges and significant energy losses and reduced compatible with high frequency switching (several hundred kilohertz)

-- Safe operation eliminating any risk of short-circuiting the source of tension,

-- Start without natural means of forcing,

-- Operation to empty (load current zero).

The static covered by the invention includes:

-- A source of tension,

-- A first switch static type ordered the Boot and blocking, with two electrodes and power electrode order,

-- A second switch static type '• ordered to boot and the blocking, with two electrodes and power electrode order, the two switches are connected in series on the source of tension and having a common point for the connection d 'burdens,

-- A first in antiparallel diode connected between the electrodes of

the first power switch - a second antiparallel diode connected to the electrodes between the second power switch,

-- A first circuit adaptation associated with the first switch to a polarization of the electrode command able to trigger changes in statements of the latter,

-- A second circuit adaptation associated with the second switch to a polarization of the electrode command able to trigger changes in statements of the latter,

-- A steering unit adapted to issue signals logical steering complementary,

-- A first detector connected state between the electrodes power switch for the first issue a status signal representative of the level of tension between those electrodes power,

-- A second detector connected state between the electrodes second power switch to issue a status signal representative of the level of tension between those electrodes power,

-- A first logical interface between the unit interspersed steering and the first circuit adaptation,

-- A second interspersed logical interface between the steering unit and the second circuit adaptation. According to this invention, the converter

- is characterized in that:

-- The first logical interface is arranged to receive the status signal from the second detector state, the interface is adapted to deliver to the first circuit adjusting a signal logic of command, carrying an order if conduction and only if:

. the steering logic signal from the steering unit corresponds to an authorization conduction, ET

. the status signal from the second detector state is representative of the state blocked both the second switch and the second diode, and carrying an order blocking if:

. the signal logic steering corresponds to an order blocking OR

. the status signal is representative of the state driver of the second switch or the state driver of the second diode,

-- The second logical interface is arranged to receive the signal condition resulting from the first detector state, the interface is adapted to deliver to the second circuit adaptive logic of a signal conduction bearer of an order of conduction if and only if:

. the steering logic signal from the steering unit corresponds to an authorization conduction,

ET. the status signal resulting from the first detector state is representative of the state blocked both the first switch and the first diode, and carrying an order blocking if:. the signal logic steering corresponds to an order blocking

OR

. the status signal is representative of the state driver of the first switch or the state driver of the first diode.

Thus, in the converter of the invention, the state detectors provide surveillance of two sets switch / diode; cross their arrangement and the logical interfaces can strictly prohibit the boot of a switch if All opposed *. switch / diode is not blocked, so that any short-circuit the source of tension is excluded m ême that any sudden blocking diodes (the state blocked a "whole switch / diode" is defined as state where the switch and the diode are blocked simultaneously, and the state driver as the state where the at least one passing).

Moreover, when the two switches are blocked, the voltage supplied by the source is divided on these two switches and each detector d 'e tat allows booting the switch opposite: the start can occur under the control of 'steering unit.

According to a preferred embodiment, the converter also: - ir a cui tr c ard and inte rc al é ent re the first logical interface and the second detector of state to introduce a delay on the status signal and the first issue to a logical interface status signal delayed

-- A cui circumstances tr etard stalled inter e ntr ela second logical interface detector and the first state to introduce a delay on the

status signal and the second issue to a logical interface status signal delayed.

Preferably, these circuits delays are adapted to introduce delays on the signals equal status in order to preserve the symmetry operation of the converter.

These circuits delays guarantee, that that is the point of operation, a commutation to boot switches turned minimal. Indeed, when a blockage is detected on a given set switch / diode, the detector circuit delay concerned differs permission boot assigned to the opposite switch, thus enabling the voltage across this switch to decline. An appropriate choice of the value of this delay allows each application to make the boot so µ s minimum voltage,

including zero tension when the load current is sufficient at the moment of the commutation.

In addition, the converter consistent with the invention advantageously includes:

-- A first-current source, impulse associated with the first switch to compel the appearance of a direct tension between its electrodes power after polarization of the electrode command said switch in the sense of deadlock,

-- A second source of current impulse associated with the second switch to force the appearance of a direct tension between its electrodes power after polarization of the electrode command said switch in the sense of stalemate.

Where the current through the load is zero or low moments of the commutations, these sources are designed to temporarily strengthen the current charge to reflect an artificially voltage between the electrodes power switch which must be blocked: this tension leads the detector state of the whole switch / diode concerned to consider the package as a secure way to authorize immediately boot the opposite switch. Moreover, where the load current is a current of diode low, the current source will block the corresponding diode (which is then bisected by a current low), the appearance of order blocking Associated switch: this ensures, in this case, the emergence of tension direct above-mentioned.

Preferably, a circuit delay is associated with each source of current

impulse to trigger the current pulse with a predetermined delay after onset of an order blocking the release of the corresponding logical interface, each current source is type current source limited tension, the delay avoids triggering a systematic current sources after each blocking order: indeed, if the load current is sufficient to cause the emergence of tension direct above-mentioned, the source Current tension will be limited

inhibited.

The following description referring to the drawings shows a preferred embodiment of a converter consistent with the invention and illustrates the allure of signals corresponding to these drawings which are part-, integral to the description:

-- Figure 1 is a block diagram of this converter - Figure 2 is a schematic electronic retailing, giving an example of achieving a current source impulse,

-- Figures 3a to 3n, 4a to 4n, and 5a to 5n are chronograms illustrating various modes of operation of the converter,

-- Figure 6 is a block diagram of an application for the invention (UPS resonance series).

The converter Basic represented as an example in Figure 1 is an arm of UPS that can be combined with one or more identical arm to feed a load CH (mono or polyphasée); elementary these converters are powered by a same source voltage (E) that the example is a continuing source amplitude e. Each converter Basic includes two switches static Kj and K2 type ordered the Boot and blockades. Each switch is connected to a diode (coasting) antiparallel D-j, D2 "KH switches and K2 may be MOS transistors, diodes D-. Dp and then being naturally integrated into these components (diodes body).

The two switches 1 and K2 are connected in series to the terminals of the source of tension E, the load being connected to star with two switches. In usual fashion, the electrode command of each switch K1 or K2 is connected to a circuit adaptation AD-j or AD2 (commonly referred to as the "circuit driver"), which ensures formatting, adaptation and the amplification signal logical command received gold-,, or2 to trigger changes in state of the switch Ki

or K2 -

The converter includes a steering unit UP which is known in itself (usually a microprocessor) and delivers two signals logical steering and complementary pil pil to control, according * implementation, the energy exchange between the source of tension E and the burden CH (eg setting the amplitude and frequency of the voltage across the load in the case of a load passive).

The signals steering pil pil and are issued on logical interfaces L0G-and L0G2 that turn those signals steering signals or command-and or2 bearer is orders blocking gold. = 0, or2 _ 0 either orders or conduction. = 1, or = 1, so as to ensure the commutation of switches K1 and K2 in conditions specific to the invention which lead to benefits detailed further.

The logical interface LOG., (L0G respectively) also receives a status signal delayed s'2,

(s respectively.,) representative of the state or blocked from all switch K / complementary diode D2

(respectively K ^ D <).

The status signal delayed s'-(respectively s' ..) is prepared by a detector state DKD2 (DKD-respectively,) followed by a delay circuit RET2 (respectively RET ").

The two circuits delays RET-,, preferably RET2 introduce a delay identical, equal to a fraction of the period of commutation of switches. Each detector state DKD. (Or DKD-) includes the example shown in Figure 1:

. a voltage comparator-COMP (or C0MP2) designed to compare the tension reverse v-(or v2) at the terminals of the corresponding diode D1 (D2) with a reference voltage v ^ j (or Vf) above saturation voltage switches static, and lower the tension e bounds of the source of tension E,

. an inverter INV1 (or INV2) arranged to receive the signal logical command from the interface logic-LOG (or L0G2) to issue a signal

complementary,

. a door AND AND logic (or AND-) arranged to receive the signal from the comparator C0MP (or C0MP2) and the complementary signal from the inverter INV1 (or INV2) to issue the status signal s - (Or s2).

The reference voltage is delivered by a generator of tension GF (or GF2) and is set in each application depending on the type of switch to a value greater than the voltage saturation of the latter, in particular order from 1.2 to 2 times the voltage saturation.

Typically, the output of each detector state, the signal century, or s2 is galvanically isolated, for example through a optocouplor.

The logical interface LOG., (L0G2 respectively) associated with the switch-K, (K2, respectively) receives a signal steering pil (pil respectively) and the status signal delayed s'2 (s respectively.,) representative of the state of the whole switch K2/diode complementary D2 (respectively-K / D.,). This interface-LOG (L0G respectively) which may be a logic gate AND issue to the circuit adaptation AD-associated, (respectively AD2) a signal logical command or, (or2 respectively), this signal carries a order conduction gold = 1 (or-respectively, = 1) if and only if: the signal logic steering pil (pil respectively) corresponds to an authorization conduction, and the status signal delayed s'2 (respectively s ') Is representative of the state blocked all switch K2/diode D2 (respectively Kj / D).

The command signal is provided with an order blocking gold = 0 (respectively or2 _. 0) in the contrary case.

Such logic, which allows you to manage the energy exchange between source and load, benefiting from the following advantages. Any violent blocking diodes is excluded because, prior to the initiation of a switch,

we ensure the blocking of the diode complementary; s'affranchit on this because of all phenomena related to these blockages violent: surge, surge, losses. Any risk of short-circuiting the source of tension is excluded because, prior to the initiation of a switch, on *- ensure that the additional switch is effectively blocked, ie it has received an order blocking and that the blocking order became

effective at the switch (a direct tension has emerged between its electrodes power).

The delay r, or r2 introduced by the delays RET-circuits, or RET2 supports booting switches under the minimum voltage and in particular, when the load current is sufficient at the moment of commutation, begin under zero voltage switches, so as to reduce losses by switching in these switches.

In addition, the converter includes associated with each set switch K / diode D, (respectively K2/D2) a current source impulse J,

(respectively-J), which is equipped with a power output connected to the cathode of the diode D, (D2 respectively) and an entry command connected to the exit of the logical interface LOG (L0G2 respectively) to generate a current pulse j, (j2 respectively) in the presence of an order blocking gold = 0 (respectively gold-= 0) from the logical interface, and thus forcing the emergence of a tension Direct v (v2 respectively) between the electrodes power switch K, (K2, respectively) after polarization of its electrode command in the sense of deadlock, the source is adapted so that this tension direct v, (respectively v2) is above the reference voltage v ^, (respectively v ^ 2) generated in the detector state DKD, (DKD respectively). A circuit delay TEMP (respectively

TEMP) is an example associated with the current source impulse J, (J2 respectively), which is kind of limited power in order to trigger the current pulse with a predetermined delay b-* (b2, respectively) after appearance on the order blocking gold = 0 (or = 0 respectively).

Preferably, the channels delays TEMP, and TEMP2 associated with the two sources J., and J-adapted to introduce delays equal b = b2. Thus, in the absence of load current i-^ or in case of failure, each current source J, J-shows a voltage direct the bounds of the switch corresponding K, K, which is more than reference voltage v ^, or Vf> 2 and allows the detector state to consider that all corresponding switch / diode is blocked: boot the additional switch is possible. These provisions allow a particular operation to get the vacuum converter (charging current ich zero) and it starts in all cases j besides, if the course load at the moment of commutation is a current diode low, the current source involves a blockage of the corresponding diode, then the emergence of a direct tension as indicated above. It preserves the operation of the converter under

the best conditions for commutation on a range of variation of the current load as widely as possible. Beyond this range, the converter is naturally self-protected against the violent blockades diodes, ever since then switch. The delay b, or b2 trigger source J, J2 or avoids it charges if the load current is sufficient to develop a voltage direct-to-terminal switches K, or K2 (voltage above the reference voltage v ^ ", Or v-.-.). Figure 2 shows an example of achieving a current source impulse J, (J2). The command signal delayed or ', resulting from delays TEMP circuit, is issued on the electrode command of a switch static Tj1 (in this instance the grille of a transistor MOS). The transistor Tj, is connected, on the one hand, a source of tension e-amplitude, which allows you to calibrate the current pulse j, on the other hand, an L-inductance - in series with a diode D **. The conduction of the transistor j, triggers an oscillation of current through the circuit formed by oscillating inductance Lj, and

capacitor 'inter-electrode power switch all K / diode D,. The Dj-diode, prevents the emergence of this oscillation if the current tension direct to the terminals of the switch-K, exceeds the tension e,. (This tension may particularly be chosen equal to the v-thresholds., *. Or vf2).

As a result, through the introduction of a delay b, the conduction of the transistor Tj, the diode DJ, inhibits spontaneously current source in case of tension between direct sufficient terminals switch K, .

Figures 3a to 3n illustrate the essential signals generated in the converter in the case of a switch in the direction of blocking the switch K2 with a load current ich low but not zero. Of these figures, it was assumed that tensions v ^., V ^.-., e, and e2 were equal (Figure 3c).

The front crossing to 0 of pil represents an order blocking the switch K2, while the passage of a 1 pil represents permission to boot the switch-K, (Figures 3a, 3b) •

We see the figure 3k that the command signal will switch to lock sequence: or2 = 0; switching signal or command, was postponed (Fig. 3f). From the moment of blocking the switch K2, the load current iQ ^ is diverted to capacitors C, and C2 intrinsic to the switches K, and K (Fig. 3 n). As a result, tensions v, and v2 evolve as shown in Figure 3c growth of tension v2 from 0 to decrease

tension v, from + e. The tension v2 pass threshold voltage v - 2 and leads the changeover comparator C0MP2 and jointly s2 signal from the detector state DKD2 (Fig. 3d). The switch K2/diode D2 is considered to be blocked (status signal s2 = 1).

The phenomenon load capacitor C2 and discharge of capacitor C-, continues. After a delay b2, the command signal delayed or'2 switches (Fig. 31) and requests the current source J2: as in this moment of solicitation, tension v is greater than the tension and

Food 'e2 of the current source J-, this source is inhibited by the diode Dj2 (Figure 3m). This illustrates the interest of avoiding delay b2 the current source impulse to charge unnecessarily. After a delay r2, the status signal delayed s'2 switches to turn and jointly signal *, or command, switches and results in an order of conduction of the switch K,: gold = 1 (Figures 3rd and 3f). The seed of this switch K, causing the collapse of tension v, and thus, tension v2 pass the value + e (Figure 3c). In dropping the tension v, falls below the threshold v *., and causes the changeover to 0 signals s state, and if, (figures 3i and 3d), which confirms the prohibition boot the switch K2. This shows the interest of delay r2 allowing a boot in the minimum voltage switch so as to reduce losses.

Figures 4a to 4n illustrate the same signals, but in the case of a commutation under load current iQ γ. = 0 (functioning vacuum). Following the order blocking the switch K2 (or2 = 0, figure 4k), tensions v, v2 and do not evolve as ich = 0. After a delay b2, the current source J2 is sought (or'2 1; figure 41). In this case, the current source is no longer inhibited and delivers a current pulse (Figure 4m), which ensures a functioning identical to previous case (growth of tension v2 and decrease the tension v ,...).

Figures 5a to 5n illustrate the same signals but in the case of a commutation under load current i α h value sufficient to ensure the boot switches turned on zero. The charge current, in this case, a value sufficient to ensure the full charge of the capacitor C (v2 = + e) and complete discharge of capacitor C, (v = 0) (figures 5c and 5n), this before that the status signal delayed s'2 switches (Figure 5th): setting conduction of the switch K, is thus turned zero after a sequence of conduction of the D-diode,.

Figure 6 is a blueprint for a converter resonance continuous series / continuous non-reversible. This converter is formed by two arm

inverter type

previous arranged a full deck. Each switch of both arms is constituted by a MOS transistor (MOS ... MOSjj); diodes are represented diodes body said transistors; capabilities represented are the intrinsic capacity to transistors. The charge is constituted by an *. T transformer whose primary is connected in series with a circuit oscillating series LC and whose secondary debit on a rectifier diode classic RED. To this figure, the party controlling each arm of UPS PCM, 2, PC ^ is identical to that described above.

Such a converter is particularly interesting to operate at high frequency (a few hundred kilohertz), this operation was viable that because device performance, particularly the reduction of losses by switching and safe operation

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3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW V. NGUYEN whose telephone number is (571)272-2081. The examiner can normally be reached on 8 HOURS M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AKM ULLAH can be reached on (571)272-2361. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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